

General Inverter Adapter Board

V3

for PED-Board®

HARDWARE

and

USER MANUAL

ped-board.com

I. Limited Warranty

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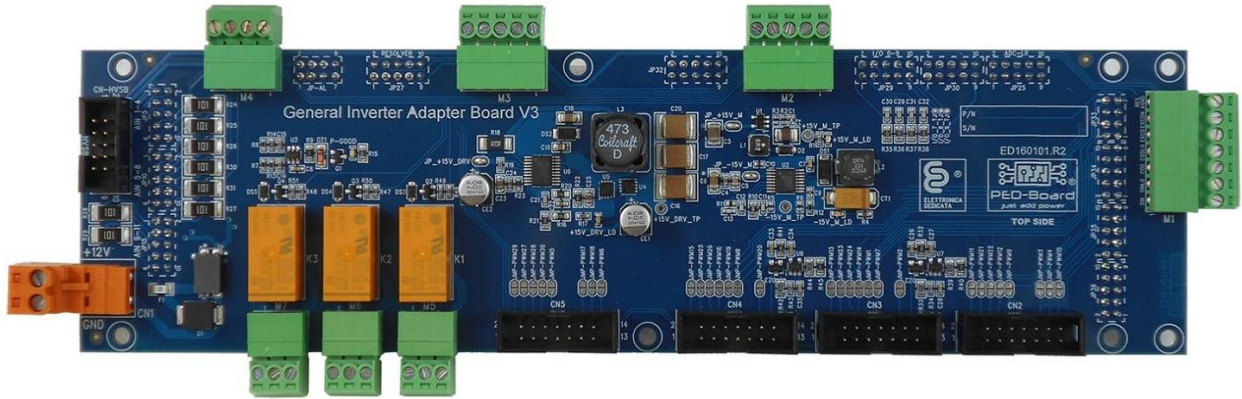
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PED-Board warrants that its hardware products will be free of defects in materials and workmanship that cause the product to fail to substantially conform to the applicable PED-Board specifications for one (1) year from the date of invoice.

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Do not use in life support and medical applications. In such cases email to support@ped-board.com

General Inverter Adapter Board – V3 • GIAB-V3



Features

- **30 x PWM channels (CN2, CN3, CN4, CN5)**
 - 0÷15 V or 0÷5V selectable voltage swing
 - Direct LED driving capability for optocoupled gate driver
- **4 x Digital I/O (CN2, CN3, CN4, CN5)**
- **8 x external current or voltage measures (M2, M3, M4)**
- **3 x differential inputs**
 - Direct connection to High Voltage Sensing Board (HVSBS-V1 and V2)
- **Resolver port (M1)**
- **2 x direct temperature measurement (CN3, CN4)**

Custom configuration for default setup for orders of 5 units or more.



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II. Electrical specifications

Recommended input voltage supply	12	V	POWER-IN
Input voltage supply range	±10%		Respect to Vin
<i>No reverse voltage protection</i>			
Input current	2.5	A	Max current at Vin
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 to 85 °C		
Operating temperature	-25 to 60 °C		
Operating humidity (IEC 60068-2-56)	10 to 90% RH, noncondensing		
Storage humidity (IEC 60068-2-56)	5 to 95% RH, noncondensing		
Maximum altitude	5000	m	
Pollution Degree (IEC 60664)	2		

Do not apply an input voltage higher than 14V at the Vin terminal with respect to GND.

- Main power supply and auxiliary connectors

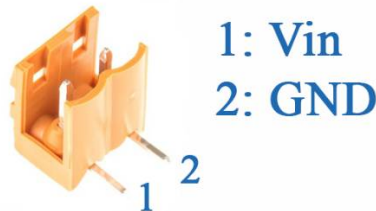


Figure 1. Pinout of the main power connector.

Power supply connector (OMNIMATE SL Weidmuller, RS code 403-998), mate connector available on Farnell with the code 1729275.

III. GIAB-V3 Connectors

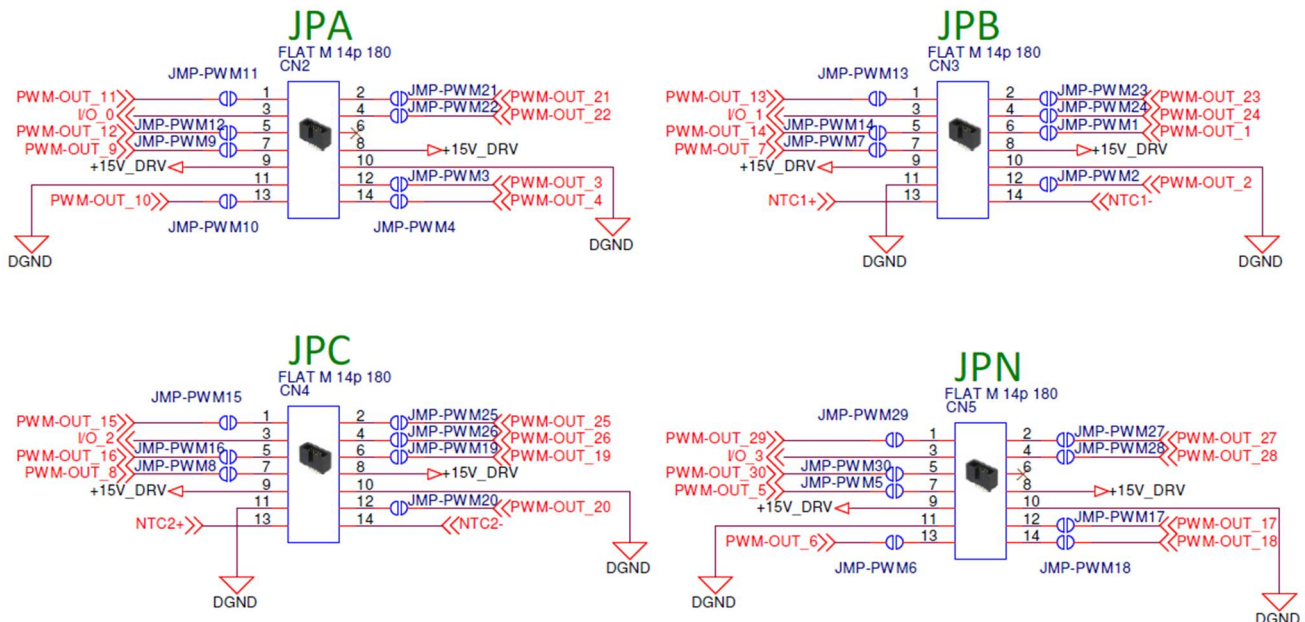


Figure 2. Pinout of CN2, CN3, CN4 and CN5.

I/O_0, I/O_1, I/O_2, I/O_3 have an on-board 3.3V pull-up resistor. Those I/Os are connected directly to the FPGA pins on the PED-Board.

+15V_DRV can be used to directly supply the gate driving circuits; consider a maximum current of 1.3A (total).

NTC1+ routed to AIN17_L, NTC2+ routed to AIN18_L. On board constant current generator is provided. Voltage is clamped to 5.1V to avoid damages to the PED-Board ADC3 system.

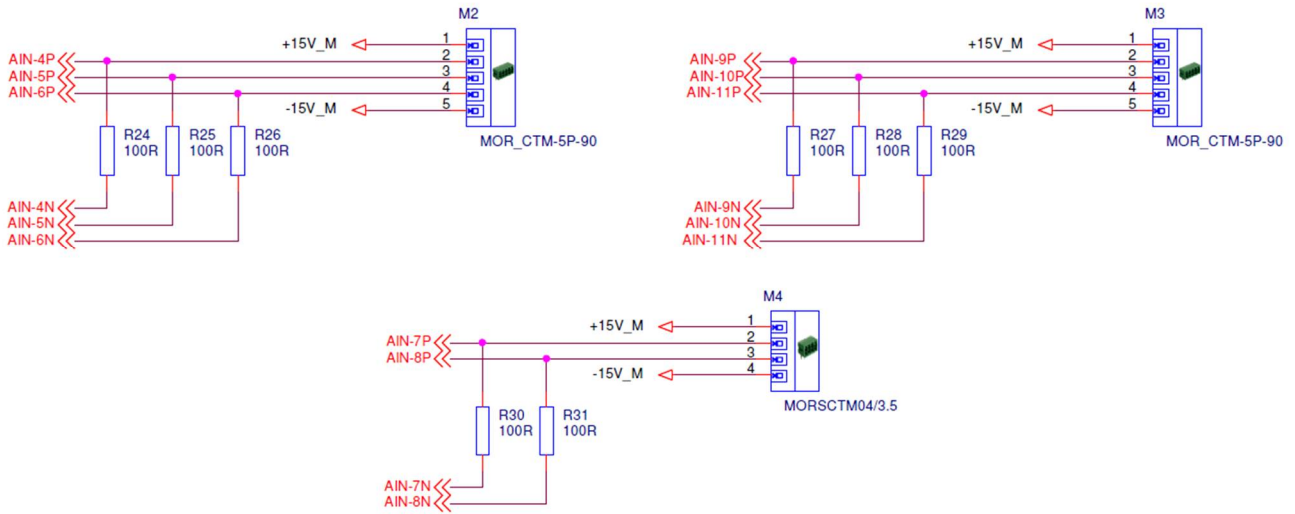


Figure 3. Connectors for external current/voltage measures. $\pm 15V$ maximum current is 500.0mA (total).

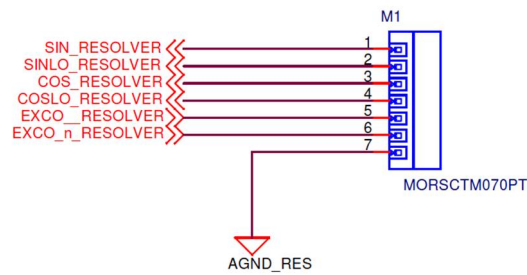


Figure 4. Resolver connector.

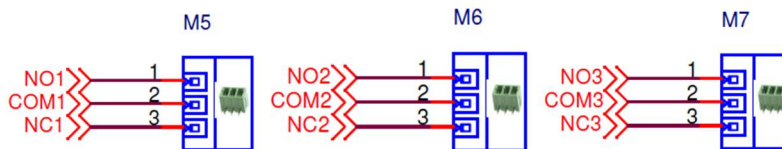


Figure 5. Relay connectors. NO: normally open. NC: normally closed. COM: common. M5 driven by I/O_4, M6 driven by I/O_5 and M6 driven by I/O_6.

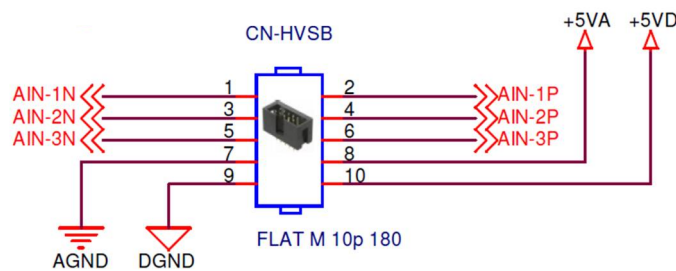


Figure 6. HVSB connector. It can be also used as additional fully differential ADC inputs.



PED-Board

just add power

GIAB-V3

r0.00

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