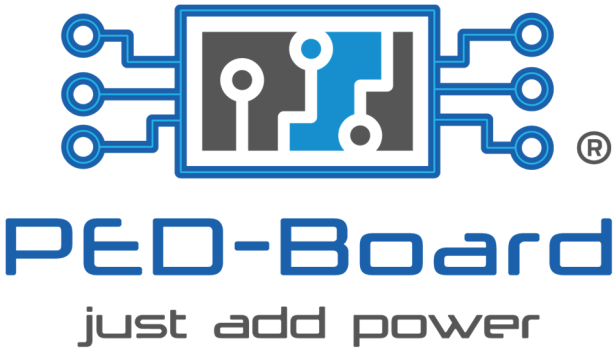

PED-Board *Mini*

for National Instruments System on Module - sbRIO-9651®

HARDWARE
and
USER MANUAL

ped-board.com

I. Limited Warranty

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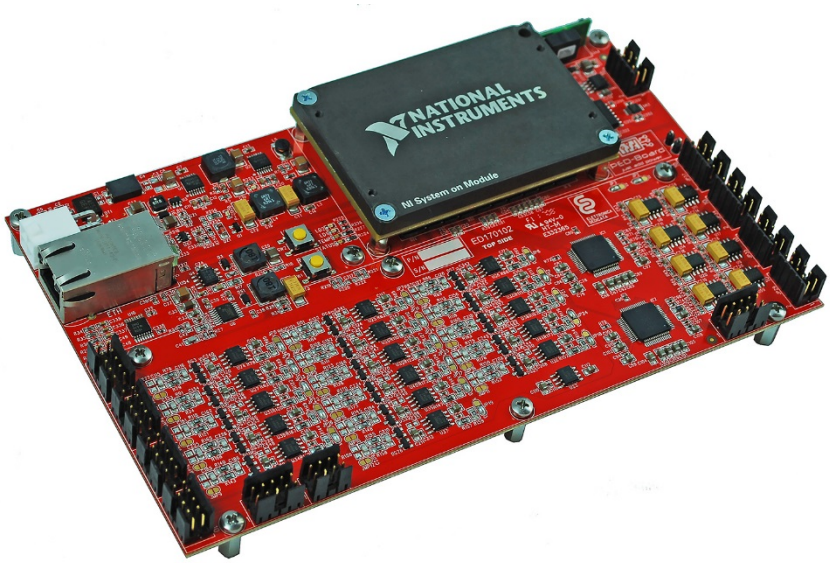
Power Electronics & Drives Board *Mini* • PED-Board *Mini*



Applications

- **Power electronics converters and electric drives**
- **Multilevel converter topologies**
- **Hybrid power systems**
- **UPS and PV converters**
- **High performance control algorithms**
- **High speed acquisitions and high throughput computation**

Fully programmable by LabVIEW®.

Peripherals supported by dedicated LabVIEW® drivers.

Fully editable demo programs.

Features

- 14-bit ADC, 8 Channels (ADC1)
  - Simultaneous sampling
  - 1.45 µs conversion time, 8 channels
  - Differential or single-ended input (each channel)
  - Bipolar (+5V/-5V) or unipolar input (0V/10V)
  - Configurable scaling circuit (each channel)
  - First order low-pass Butterworth active filter with configurable cut-off frequency and impedance matching circuit
- 14-bit ADC, 8 Channels (ADC2)
  - Simultaneous sampling
  - 1.45 µs conversion time, 8 channels
  - Differential or single-ended input (each channel)
  - Bipolar (+5V÷-5V) or unipolar input (0V÷10V)
  - Configurable scaling circuit (each channel)
  - First order low-pass Butterworth active filter with configurable cut-off frequency and impedance matching circuit
- 12-bit DAC, 4 Channels (DAC)
  - Digital-to-analog converter with 5 µs settling-time
  - High voltage isolation, no ground loops
  - 0V÷5V output range
- 1 x CAN-bus
  - 2.0A and 2.0B support, up to 1 Mbit/s
- 1 x isolated digital output, 5V standard
- 18 x Digital I/O, 3.3V standard (Digital I/O)
  - Hall-effect position sensors interface
  - Encoder interface
  - Relay control
  - Additional PWM
  - General purpose I/O
  - Additional CAN controller
  - 5V and 3.3V supply available for buffers and transceivers
- 5 x buffered Digital I/O, 5V standard (Digital I/O)
  - Encoder and Digital I/O port
  - On-board pull-up and noise reduction circuit
  - Buffer with bidirectional capabilities and autosense
- 16 x PWM channels (PWM)
  - 0÷15 V or 0÷5V selectable voltage swing
  - Direct LED driving capability for optocoupled gate driver
  - Additional PWM channels available through the Digital I/O interface
- 1 x 10/100/1000 base-T Ethernet port
  - Auto-negotiated, half/full-duplex
  - Programming, debugging and operation
- 1 x RS-485
  - half-duplex and full-duplex communication
- 12V main supply

Custom configuration for scaling circuits, filtering and default setup for orders of 5 units or more.

Functional block diagram

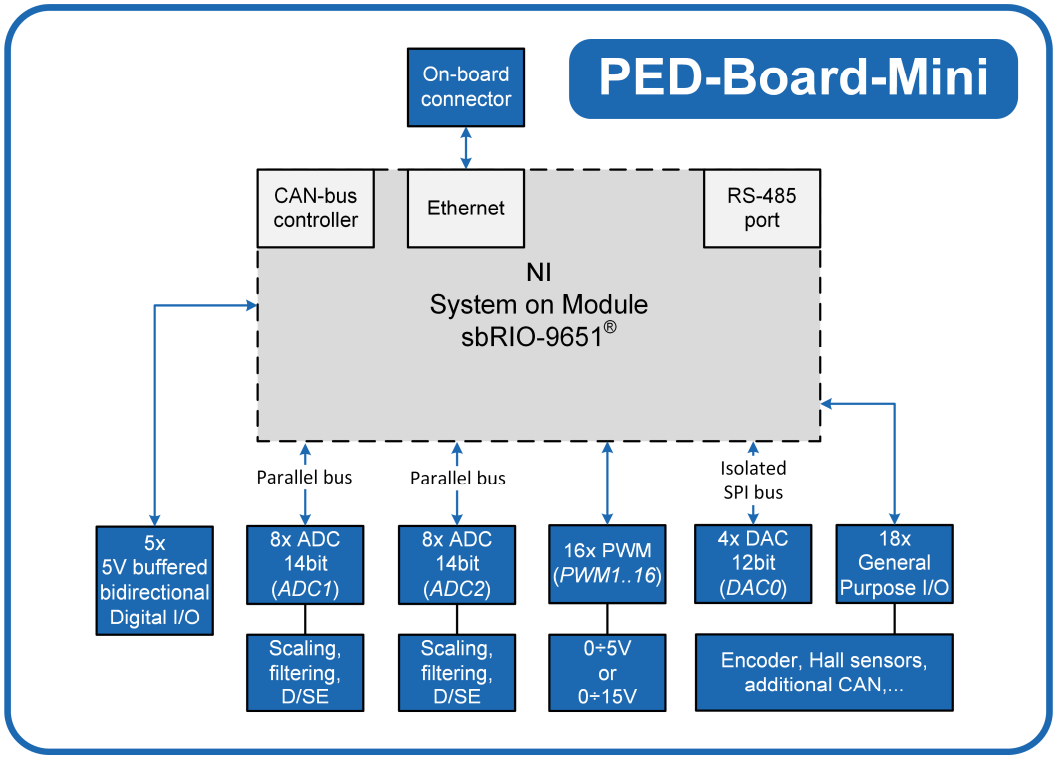


Table of contents

II. Electrical specifications

Recommended input voltage supply	12	V	Vin - DC
Input voltage supply range	±7%		Respect to Vin
No reverse voltage protection			
Input current	2.2	A	Max current at Vin
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 to 85 °C		
Operating temperature	-25 to 60 °C		
Operating humidity (IEC 60068-2-56)	10 to 90% RH, noncondensing		
Storage humidity (IEC 60068-2-56)	5 to 95% RH, noncondensing		
Maximum altitude	5000	m	
Pollution Degree (IEC 60664)	2		
Analog inputs AINx (ADC1, ADC2) max voltage	±10	V	

Do not apply an input voltage higher than 14V at the Vin terminal with respect to GND.

- *Main power supply and auxiliary connectors*

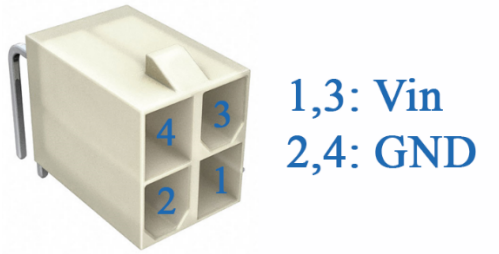


Figure 1. Pinout of the main power connector.

Mate connector DIGIKEY code WM3701-ND, manufacturer Molex. Pin DIGIKEY code WM2501-ND, manufacturer MOLEX.
PED-Board *Mini* is equipped with an auxiliary power connector, which can be used also from the application specific Adapter Board. Pinout is reported in Figure 2, where channels referred to AGND (+5V, ±10.4V) can provide up to 100mA each one, whereas the 12V link up to 350mA.

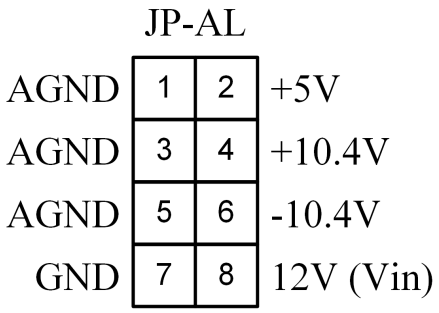


Figure 2. Connector for the auxiliary supply.

III. Analog-to-Digital converters

Analog to digital interface is based on three separate converters named respectively ADC1 and ADC2. ADC1 and ADC2 have their dedicated scaling-filtering input circuit, with detailed explanation illustrated below.

A. ADC1 interface

Analog-to-Digital Converter 1 (ADC1) is composed by 8 channels with simultaneous sampling capability and a resolution of 14 bit. Sampling and conversion for the 8 channels take around 1.45 µs being capable of theoretically 600 kS/s.
Filtering is performed by a fully configurable differential or single-ended input stage with a first order Butterworth type active filter (RC filter with impedance matching circuit). Proper measure scaling can be accomplished changing resistor values in the input stage. Block scheme of ADC1 acquisition chain is shown in Figure 3.

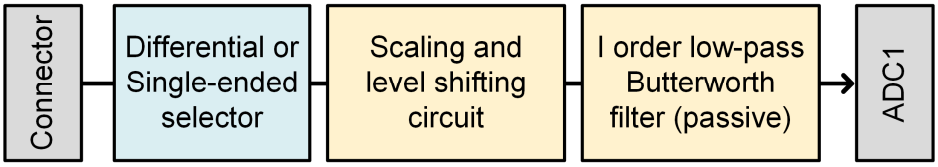


Figure 3. ADC1 measurement chain.

Level shifting circuit is provided to manage both unipolar and bipolar measures. Analog input voltage range is ±5V or 0V to +10V at the input. Provided differential scaling circuit has an input to output gain G_{SC} equals to

$$G_{SC} = \frac{V_{out}}{V_{in}} = 0.0997\left(1 + \frac{R_{g1}}{R_{g2}}\right) \quad (1)$$

where each resistor can be found according to Table 1.
Each analog input can be configured as fully differential or single-ended according to the system requirement. This can be done by JMPx footprint, where x stands for the channel (1…8). When single-ended measure is required a short circuit must be provided, whereas open circuit stands for differential input. Detailed information are reported in Table 1. Default configuration is for fully differential measures, JMPx open.
Level shifting circuit can be enabled for each analog channel. Bipolar measures are allowed to be sent to ADC in the range of ±5V at the ADC input. In this case 0V input corresponds to 0V at the ADC pin. When unipolar input is desired, 0V at the input terminal corresponds to -5V at the ADC terminal allowing the usage of the converter full scale without resolution deterioration. Selector vs. input is shown in Table 1. When pin 1 and pin 2 are shorted together, resulting measure is unipolar, whereas pin 2 shorted to pin 3 results in bipolar input.

Table 1 – ADC1 configuring information

			Single-ended / Differential		Unipolar / Bipolar	
Analog input	**R_{g1}**	**R_{g2}**	**Closed**	**Open (default)**	**1-2 unip.**	**2-3 bip.**
AIN-1P / AIN-1N	R_{78}	R_{80}	JMP1		JP6 (2-3 default)	
AIN-2P / AIN-2N	R_{83}	R_{85}	JMP2		JP7 (2-3 default)	
AIN-3P / AIN-3N	R_{88}	R_{90}	JMP3		JP8 (2-3 default)	
AIN-4P / AIN-4N	R_{93}	R_{95}	JMP4		JP9 (2-3 default)	
AIN-5P / AIN-5N	R_{110}	R_{112}	JMP5		JP11 (2-3 default)	
AIN-6P / AIN-6N	R_{115}	R_{117}	JMP6		JP12 (2-3 default)	
AIN-7P / AIN-7N	R_{120}	R_{122}	JMP7		JP13 (1-2 default)	
AIN-8P / AIN-8N	R_{125}	R_{127}	JMP8		JP14 (1-2 default)	

Default values: R_{g1}=29.4kΩ, R_{g2}=3.24kΩ with 1% accuracy, resulting in a gain of 1.014[1].

ADC output data format is in two-complement, independently from the Unipolar/Bipolar scale selection. Retrieved data specifications are highlighted in Table 2. Accordingly, being the ADC resolution equals to 14-bits, resulting data DB[15:14] are set to zero for positive input voltage and one when negative voltage is applied.

Improved code efficiency and reduced FPGA occupancy can be obtained when 14-bits data input is considered using fixed-point signed data type, avoiding to read DB[15:14].

Table 2 – ADC output data format

Description	Input voltage value at the ADC pin	Binary and hexadecimal code DB[15:0]
Positive full scale	+5V	0b ~~00~~01 111 1111 1111 0x 1FFF
Negative full scale	-5V	0b ~~11~~10 0000 0000 0000 0x E000

The pinout of the ADC1 input connector is shown in Figure 4. Each analog input must be connected between the related input P and N. Signal in converted considering the voltage difference P-N (maximum voltage on each pin is 10V).

[1] *Custom configuration available for orders of 5 or more units.*

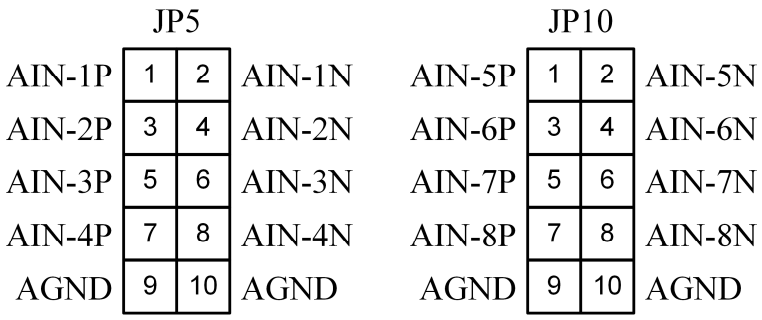


Figure 4. ADC1 connectors.

- *ADC1 filtering section*

ADC1 filtering section is accomplished by a simple first order resistive-capacitive low-pass filter having an impedance matching circuit at its output. Related circuit scheme is shown in Figure 5
Filter cut-off frequency can be selected by choosing the value of the capacitor C_f according to the following expression:

$$F_{coADC1}[Hz] = \frac{1}{2\pi 10^4 C_f[F]}$$

Filtering capacitor related to each analog input channel is accomplished by the parallel connection of two separated capacitors. PED-Board *Mini* components designator are reported in Table 3.

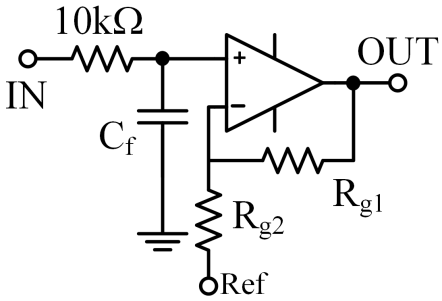


Figure 5. General electrical scheme of the II order Butterworth filter.

Table 3 – ADC filtering capacitor (default: not mounted)[2]

Analog input	C_f
AIN-9P / AIN-9N	C_{340}
AIN-10P / AIN-10N	C_{341}
AIN-11P / AIN-11N	C_{342}
AIN-12P / AIN-12N	C_{343}
AIN-13P / AIN-13N	C_{344}
AIN-14P / AIN-14N	C_{345}
AIN-15P / AIN-15N	C_{346}
AIN-16P / AIN-16N	C_{347}

B. ADC2 interface

ADC2 interface is similar to the previously depicted ADC1, except for the low-pass filtering path that is composed by a simple RC filter with impedance matching circuit. Signal conditioning chain is highlighted in Figure 6. Input circuit devoted to scaling and level shifting exhibits the same gain as shown in (1). Each analog input can be configure as single-ended or differential by connecting proper board pads. Moreover, all channels can be configured independently for unipolar or bipolar input. Detailed information are available in Table 4.

[2] *Custom configuration available for orders of 5 or more units.*

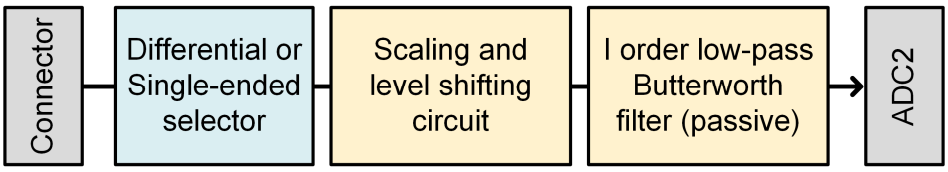


Figure 6. ADC2 measurement chain.

Table 4 – ADC2 configuring information

			Single-ended / Differential		Unipolar / Bipolar	
Analog input	**R_{g1}**	**R_{g2}**	**Closed**	**Open (default)**	**1-2 unip.**	**2-3 bip.**
AIN-9P / AIN-9N	R_{142}	R_{144}	JMP9		JP16 (2-3 default)	
AIN-10P / AIN-10N	R_{147}	R_{149}	JMP10		JP17 (2-3 default)	
AIN-11P / AIN-11N	R_{152}	R_{154}	JMP11		JP18 (2-3 default)	
AIN-12P / AIN-12N	R_{157}	R_{159}	JMP12		JP19 (2-3 default)	
AIN-13P / AIN-13N	R_{162}	R_{164}	JMP13		JP21 (2-3 default)	
AIN-14P / AIN-14N	R_{167}	R_{169}	JMP14		JP22 (2-3 default)	
AIN-15P / AIN-15N	R_{172}	R_{174}	JMP15		JP23 (1-2 default)	
AIN-16P / AIN-16N	R_{177}	R_{179}	JMP16		JP24 (1-2 default)	

Default values: R_{g1}=29.4kΩ, R_{g2}=3.24kΩ with 1% accuracy, resulting in a gain of 1.014.

ADC2 inputs are available on the PED-Board *Mini* with reference to the pinout shown in Figure 7.

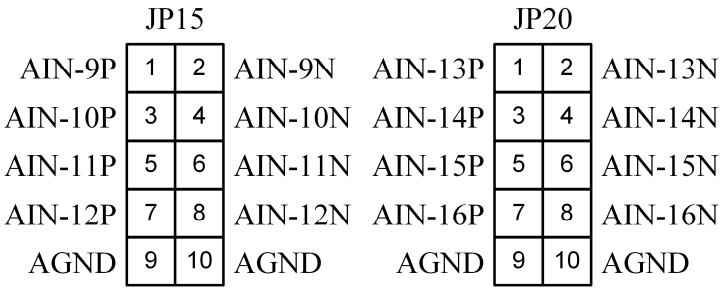


Figure 7. ADC2 connectors.

- *ADC2 filtering section*

ADC2 filtering section is accomplished by a simple first order resistive-capacitive low-pass filter having an impedance matching circuit at its output. Related circuit scheme is shown in Figure 8. Filter cut-off frequency can be selected by choosing the value of the capacitor C_f according to the following expression:

$$F_{coADC2}[Hz] = \frac{1}{2\pi 10^4 C_f[F]} \quad (2)$$

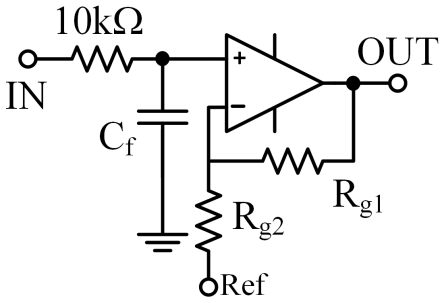


Figure 8. ADC2 filtering and scaling stage.

Filtering capacitor related to each analog input channel is accomplished by a single capacitor having 0805 footprint. PED-Board *Mini* components designators are reported in Table 5.

Table 5 – ADC filtering capacitor (default: not mounted)[3]

Analog input	C_f
AIN-9P / AIN-9N	C_{348}
AIN-10P / AIN-10N	C_{349}
AIN-11P / AIN-11N	C_{350}
AIN-12P / AIN-12N	C_{351}
AIN-13P / AIN-13N	C_{352}
AIN-14P / AIN-14N	C_{353}
AIN-15P / AIN-15N	C_{354}
AIN-16P / AIN-16N	C_{355}

IV. PWM channels (Buffered Digital Outputs)

Up to 16 independent PWM channels are provided through the connectors JP34 and JP35 having the detailed pinout of Figure 9. Each connector that is composed by 8 PWM, can be configured to provide 0÷15 V or 0÷5 V voltage swing. When 0÷5V is selected, the PWM pin can drive directly the input LED of a classical opto-coupled gate driver, such as ACPL-333J or HCPL-316.

Voltage selection can be configured by JP2 and JP3 selectors. Connecting pin 2 to pin 1, each group is supplied from the on-board +5V with 15mA continuous current capability on each PWM output. Whereas connecting pin 2 to pin 3, PWM voltage swing is 0÷15V with 5mA continuous current on each PWM channel. JP2 controls PWM1 to PWM8, JP3 is related to PWM9 to PWM16, as summarized in Table 6. PWM buffer circuit is non-inverting.

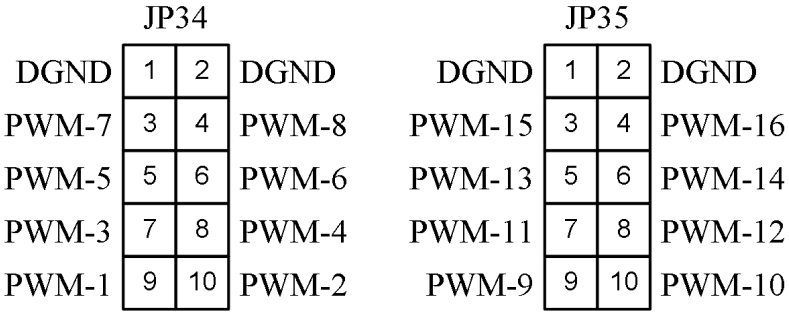


Figure 9. PWM connectors.

Table 6 – PWM voltage swing configuration[4]

	PWM1…PWM8 (JP2)	PWM9…PWM16 (JP3)
Position 1-2	+5 V (default)	+5 V (default)
Position 2-3	+15 V	+15 V

Additional PWM outputs can be achieved from the *Digital I/O* pins, implementing the voltage and current driving circuits directly on the application specific Adapter Board.

[3] *Custom configuration available for orders of 5 or more units.*
[4] *Custom configuration available for orders of 5 or more units.*

When each PWM channel needs to be controlled by a dedicated algorithm, NI sbRIO-9651 pins can be directly accessed using the following information (Table 7).

Table 7 – PED-Board *Mini* and sbRIO-9651 PWM pin routing

PED-Board *Mini*	sbRIO-9651	PED-Board *Mini*	sbRIO-9651
PWM-1	DIO_33_N	PWM-9	DIO_32_N
PWM-2	DIO_33	PWM-10	DIO_32
PWM-3	DIO_30	PWM-11	DIO_31
PWM-4	DIO_37_MRCC	PWM-12	DIO_38_MRCC
PWM-5	DIO_29	PWM-13	DIO_28_N
PWM-6	DIO_29_N	PWM-14	DIO_31_N
PWM-7	DIO_36_SRCC	PWM-15	DIO_37_N
PWM-8	DIO_36_N	PWM-16	DIO_39_N

V. Digital-to-Analog interface and isolated digital output

Digital to analog interface is based on a fast, low settling time converter with SPI interface. Output voltage, which swings from 0V to +5V, is isolated from the board ground, allowing to drive directly any output circuit avoiding ground loops. DAC resolution is 12 bit, starting from 0 to 4095 where the full output voltage is available. DAC connector shown in Figure 10 provide also one isolated digital output channel, DO-ISO (0÷5V standard). DAC and DO-ISO are on the same ground.

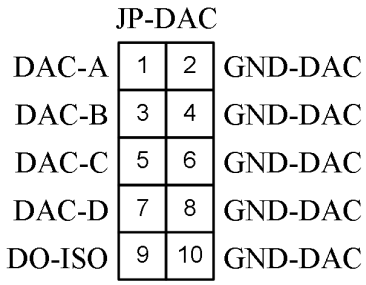


Figure 10. Connector for DAC and Digital-Out pin.

VI. CAN-bus and RS485 port

PED-Board *Mini* is not equipped with an on-board CAN transceiver. Provided CAN controller can work with a data rate up to 1 Mbit/s. LabVIEW CLIP can straightforwardly realize the CAN controller if needed. However, it takes some FPGA resources resulting in an average estimation around 5.9% of Slice Registers, 12.5% of Slice LUTs and 10% of Block RAMs. No DSP48s resources are taken to implement the CAN controller. CAN controller has been tested using the isolated transceiver ADM3053 from Analog Devices.
When CAN communication is not needed, FPGA space can be saved by removing the CAN controller from the generated CLIP. CLIP generation requires the information concerning the sbRIO-9651 pins to be used as CAN TX and RX. CAN controller should be generated according to the information reported in Table 8.

Table 8 - Pin routing between the CAN-Bus transceiver and the sbRIO-9651

PED-Board *Mini*	sbRIO-9651
CAN_TX	DIO_8
CAN_RX	DIO_9

- *II CAN controller*

A second CAN-bus controller can be implemented by the LabVIEW CLIP generator and it will be available to the Digital I/O pins. The required transceiver must be placed directly on the *Adapted Board*.
RS485 port can be generated by the LabVIEW CLIP Generator. PED-Board *Mini* is not equipped with an on-board transceiver, which should be placed on an additional external board. RS485 CLIP can be generated according to the pin routing shown in Table 9. RS485 port has been tested using the isolated transceiver such as the ADM2587 from Analog Devices.

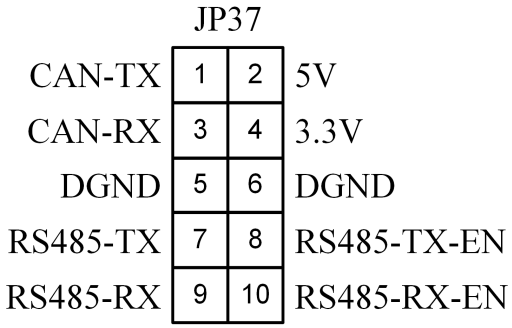


Figure 11. CAN-bus and RS485 connector.

Table 9 – Pin routing between the RS485 transceiver and the sbRIO-9651

PED-Board *Mini*	sbRIO-9651	
RS485-TX-EN	DIO_11	Transceiver TX enable pin
RS485-TX	DIO_12	Transceiver TX pin
RS485-RX	DIO_14	Transceiver RX pin
RS485-RX-EN	DIO_15_MRCC	Transceiver RX enable pin

VII. Digital I/O

Additional digital I/O pins are available through JP29 and JP30 connectors that allow to route those pins directly to the *Adapter Board*. Connectors' pinout is highlighted in Figure 12. Digital I/O are directly connected to the ZYNQ-7020 pins, refers to the Xilinx device data-sheet for the electrical specifications.

Provided additional Digital I/O pins are directly connected to the sbRIO-9651 FPGA pins. According to the National Instruments sbRIO-9651 data-sheet, the relation between the PED-Board *Mini* and sbRIO-9651 pins is as in Table 10.

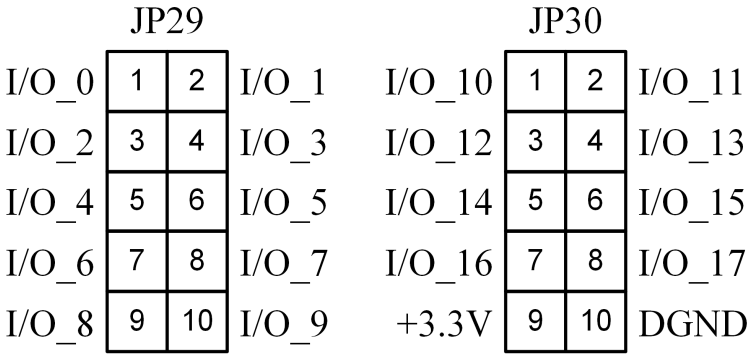


Figure 12. Digital I/O connectors.

Table 10. PED-Board *Mini* vs. sbRIO-9651 digital I/O pins

PED-Board *Mini*	sbRIO-9651	PED-Board *Mini*	sbRIO-9651
I/O_0	DIO_25_N	I/O_9	DIO_20
I/O_1	DIO_0	I/O_10	DIO_23_N
I/O_2	DIO_25	I/O_11	DIO_21_N
I/O_3	DIO_1	I/O_12	DIO_24
I/O_4	DIO_22	I/O_13	DIO_21
I/O_5	DIO_19	I/O_14	DIO_24_N
I/O_6	DIO_22_N	I/O_15	DIO_43_N
I/O_7	DIO_20_N	I/O_16	DIO_47
I/O_8	DIO_23	I/O_17	DIO_43

C. Hall sensors interface and Encoder port

PED-Board *Mini* is equipped with a digital interface for glue less connection of low-resolution hall-effect position sensors. These can be connected to the pins provided by the Digital I/O port, JP29 and JP30. As shown in Figure 12, non-isolated

+3.3V supply is provided, which can be used to directly fed hall-sensors and encoders with a maximum available current of 100mA. Additional connector for 5V general purpose I/O is JP36 having the pinout highlighted in Figure 13. Digital pins of JP36 are buffered bidirectional with direction autosense and 5V logic. The input stage of each I/O pin of JP36 is summarized in Figure 14, where the electrical characteristics can be found considering the TI TXB0106PWR.

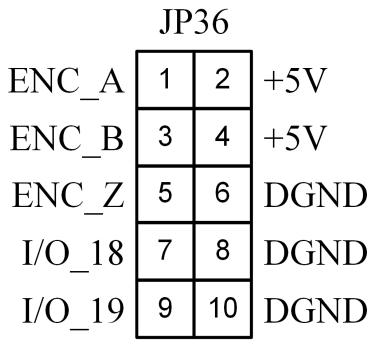


Figure 13. Digital I/O connector.

Table 11. PED-Board *Mini* vs. sbRIO-9651 digital I/O pins

PED-Board *Mini*	sbRIO-9651
ENC_A	DIO_64
ENC_B	DIO_64_N
ENC_Z	DIO_65
I/O_18	DIO_48
I/O_19	DIO_44

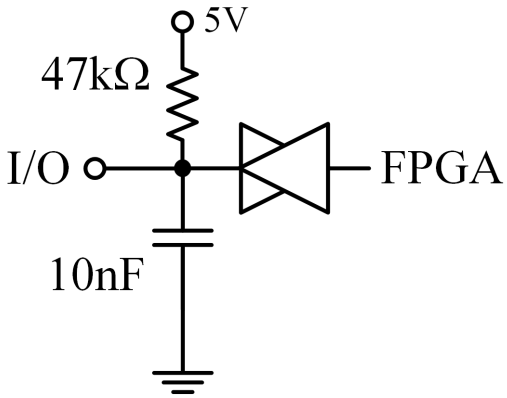


Figure 14. JP36 input circuit.

VIII. Status and User LEDs, User button and Reset

PED-Board *Mini* is equipped with three LEDs related to the sbRIO-9651 operation, POWER (green), STATUS (yellow) and TEMP (red). Please refer to the National Instruments System-On-Module data-sheet for detailed explanation.

Additional user LEDs are provided, which can be controlled directly from the sbRIO-9651: LED1 (green) connected to the pin DIO_75 and LED2 (green) connected to DIO_81.

NI sbRIO-9651 can be reset by pressing SW1. SW2 can be used as user switch, having normally low state. It is connected to the DIO_87_SRCC pin of the sbRIO-9651 board.

IX. Mechanical dimensions

PED-Board *Mini* size is 187.5mm x 112.7mm.

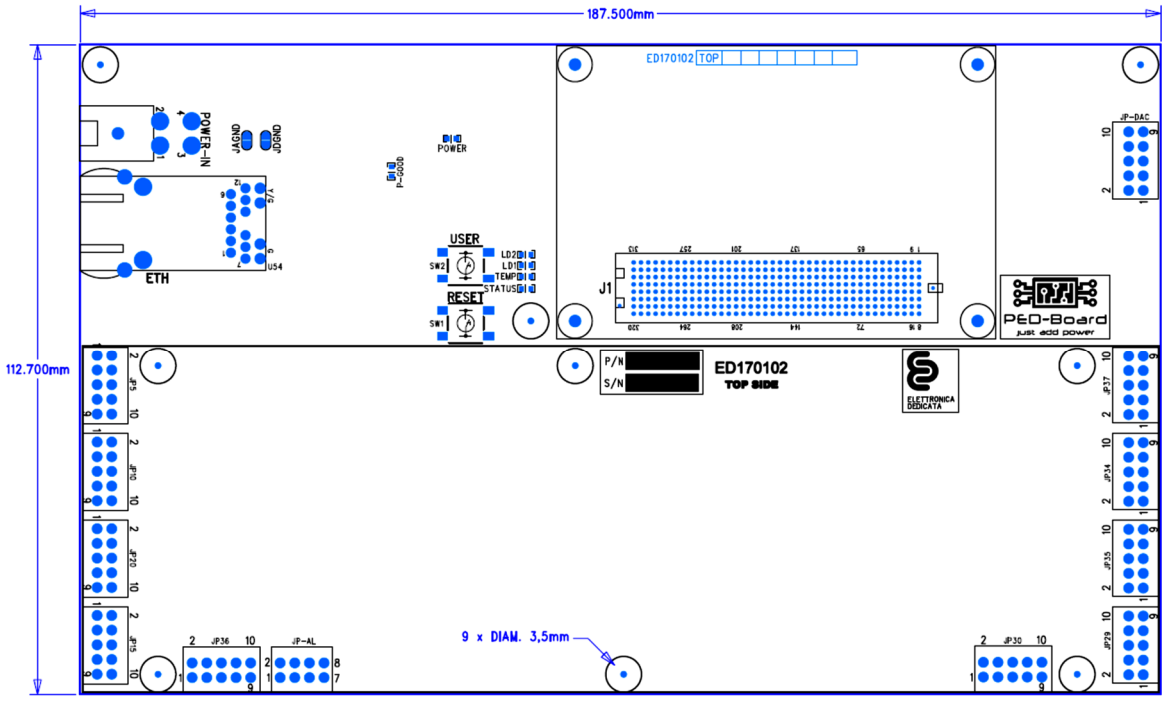


Figure 15. PED-Board *Mini* mechanics.

Detailed mechanical information can be found on-line in the download section.

When needed, the application specific Adapter Board should be placed above the board-to-board connectors, i.e. in the PED-Board *Mini* bottom rectangle shown in Figure 15.

X. Connectors selection

PED-Board *Mini* can be ordered with two different connectors. The classical strip-line for board-to-board assembly, and a fast-plug removable connectors. Connectors information are reported as follows.

Designator	Type-1 (board-to-board)		Type-2 (fast plug)	
JP-AL	2x4 Strip-line (female) RS 681-6836	Mating male MOUSER 855-M20-9980446	Digikey 609-2424-ND	Mating, female Digikey 609-2381-ND Contact Crimp Digikey 609-4536-1-ND
JP34, JP35, JP5, JP10, JP15, JP20, JP-DAC, JP37, JP29, JP30, JP36	2x5 Strip-line (female) Mouser 855-M20-7830546	Mating, male MOUSER 855-M20-9980546	Digikey 609-2425-ND	Mating, female Digikey 609-2382-ND Contact Crimp Digikey 609-4536-1-ND
	Type-1 (board-to-board)		**Type-2 (fast plug)[5]**	
				
	JP-AL	JP34,…	JP-AL	JP34,…

[5] *Available also from RS-Components and Mouser*

Revision history

Date	Rev #	
2017/09/06	1.02	JP34, PWM-2 and PWM-4 were flipped JP26 changed to JP-DAC as reported on the board
2017/03/31	1.01	C. Hall sensors interface and Encoder port (update)
2017/03/07	1.00	Preliminary H&U Manual released

Contacts

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