PED-Board

just add power

Power Electronics & Drives Board

for National Instruments System on Module - sbRIO-9651®

HARDWARE and USER MANUAL

ped-board.com

I. Limited Warranty

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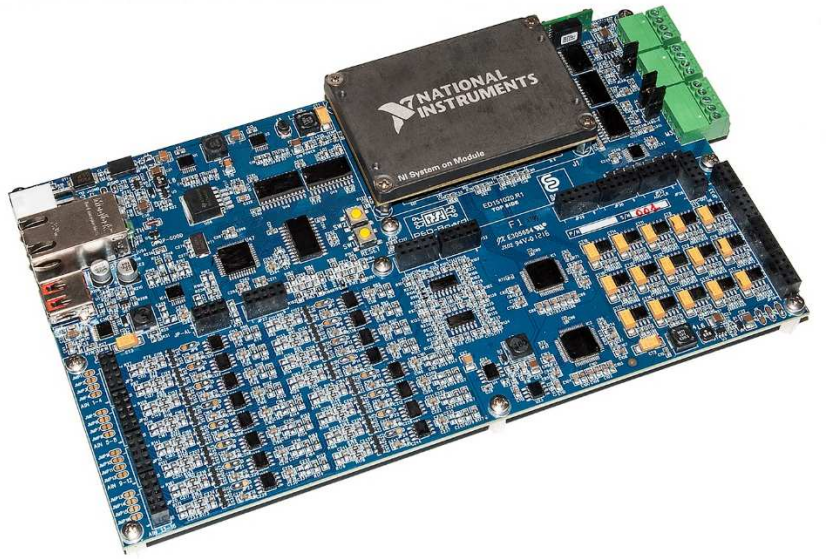


Applications

- **Power electronics converters and electric drives**
- **Multilevel converter topologies**
- **Hybrid power systems**
- **UPS and PV converters**
- **High performance control algorithms**
- **High speed acquisitions and high throughput computation**

Fully programmable by LabVIEW®.

Peripherals supported by dedicated LabVIEW® drivers.

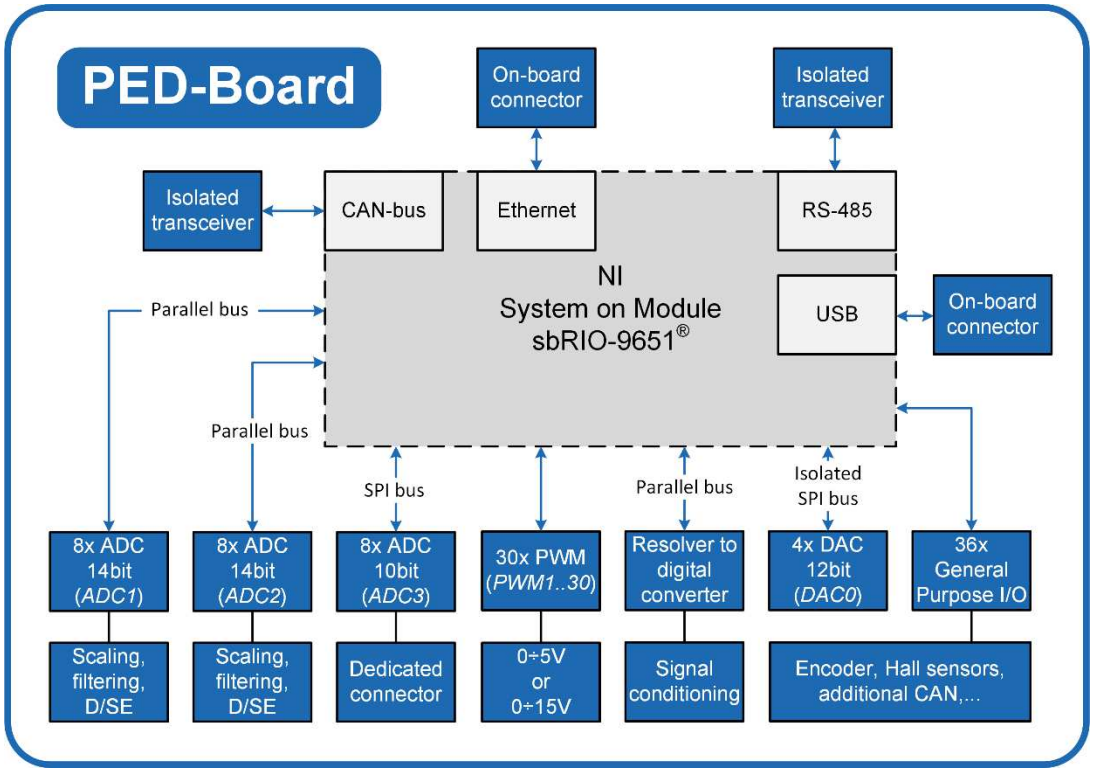
Fully editable demo programs.

Features

- **30 x PWM channels**
  - **0÷15 V or 0÷5V selectable voltage swing**
  - **Direct LED driving capability for optocoupled gate driver**
  - **Additional PWM channels available through the Digital I/O interface**
- **14-bit ADC, 8 Channels**
  - **Simultaneous sampling**
  - **1.45 µs conversion time, 8 channels**
  - **Differential or single-ended input (each channel)**
  - **Configurable scaling circuit (each channel)**
  - **Second order low-pass Butterworth active filter with configurable cut-off frequency**
- **14-bit ADC, 8 Channels**
  - **Simultaneous sampling**
  - **1.45 µs conversion time, 8 channels**
  - **Differential or single-ended input (each channel)**
  - **Configurable scaling circuit (each channel)**
  - **First order low-pass Butterworth active filter with configurable cut-off frequency and impedance matching circuit**
- **10-bit ADC, 8 Channels**
  - **Up to 200 kS/s**
- **12-bit DAC, 4 Channels**
  - **Digital-to-analog converter with 10 µs settling-time**
  - **Isolated, no ground loops**
- **Resolver interface**
  - **Fully configurable electrical interface**
  - **Speed and position measurement**
  - **Resolver fault detection**
- **36 x Digital I/O**
  - **Hall-effect position sensors interface**
  - **Encoder interface**
  - **Relay control**
  - **Additional PWM**
  - **General purpose I/O**
  - **Additional CAN controller**
- **Ethernet (programming, debugging and operation)**
- **1 x RS-485**
  - **Isolated transceiver**
  - **half-duplex and full-duplex communication**
- **1 x CAN-bus**
  - **2.0A and 2.0B support**
  - **Isolated transceiver**
  - **Up to 1 Mbit/s**
- **USB port**

Custom configuration for scaling circuits, filtering and default setup for orders of 5 units or more.

Functional block diagram



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II. Electrical specifications

Recommended input voltage supply	12	V	Vin - DC
Input voltage supply range	±10%		Respect to Vin
No reverse voltage protection			
Input current	2.5	A	Max current at Vin
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 to 85 °C		
Operating temperature	-25 to 60 °C		
Operating humidity (IEC 60068-2-56)	10 to 90% RH, noncondensing		
Storage humidity (IEC 60068-2-56)	5 to 95% RH, noncondensing		
Maximum altitude	5000	m	
Pollution Degree (IEC 60664)	2		
Analog inputs AINx (ADC1, ADC2) max voltage	±8 0…+8	V	When channel is configured as bipolar When channel is configured as unipolar
Analog inputs AINx (ADC3) max voltage	0…+5	V	

Do not apply an input voltage higher than 14V at the Vin terminal with respect to GND.

- *Main power supply and auxiliary connectors*

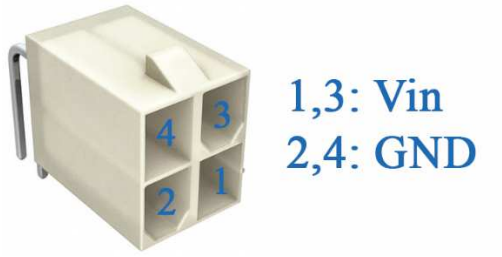

Figure 1. Pinout of the main power connector.

Mate connector DIGIKEY code WM3701-ND, manufacturer Molex. Pin DIGIKEY code WM2501-ND, manufacturer MOLEX.
PED-Board is equipped with an auxiliary power connector, which can be used also from the application specific Adapter Board. Pinout is reported in Figure 2, where channels referred to AGND (+5V, ±9V) can provide up to 100mA each one, whereas the 12V link up to 350mA.

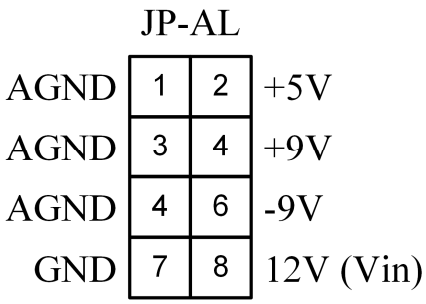

Figure 2. Connector for the auxiliary supply.

III. Analog-to-Digital converters

Analog to digital interface is based on three separate converters named respectively ADC1, ADC2 and ADC3. ADC1 and ADC2 have their dedicated scaling-filtering input circuit, with detailed explanation illustrated below. ADC3 input are provided with any interfacing hardware leaving to the final user their usage: temperature sensors, etc…

A. ADC1 interface

Analog-to-Digital Converter 1 (ADC1) is composed by 8 channels with simultaneous sampling capability and a resolution of 14 bit. Sampling and conversion for the 8 channels take around 1.45µs being capable of 600kS/s.
Filtering is performed by a fully configurable differential or single-ended input stage with a second order Butterworth type active filter. Proper measure scaling can be accomplished changing resistor values in the input stage, whereas filtering section exhibit a gain equals to one. Block scheme of ADC1 acquisition chain is shown in Figure 3.

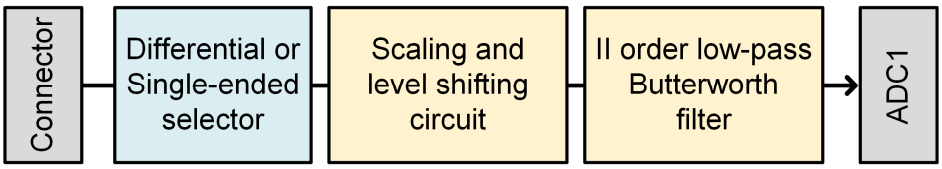

Figure 3. ADC1 measurement chain.

Level shifting circuit is provided to manage both unipolar and bipolar measures. Analog input voltage range is ±8 V or 0 V to +8 V at the input; whereas maximum operating voltage on the ADC input is ±5V.
Provided scaling circuit has an input to output gain G_{SC} equals to

$$G_{SC} = \frac{V_{out}}{V_{in}} = 0.09967\left(1 + \frac{R_{g1}}{R_{g2}}\right) \quad (1)$$

where each resistor can be found according to Table 1.
Each analog input can be configured as fully differential or single-ended according to the system requirement. This can be done by JMPx footprint, where x stands for the channel (1…8). When single-ended measure is required a short circuit must be provided, whereas open circuit stands for differential input. Detailed information are reported in Table 1. Default configuration is for fully differential measures, JMPx open.
Level shifting circuit can be enabled for each analog channel. Bipolar measures are allowed to be sent to ADC in the range of ±5V at the ADC input. In this case 0V input corresponds to 0V at the ADC pin. When unipolar input is desired, 0V at the input terminal corresponds to -5V at the ADC terminal allowing the usage of the converter full scale without resolution deterioration. Selector vs. input is shown in Table 1. When pin 1 and pin 2 are shorted together, resulting measure is unipolar, whereas pin 2 shorted to pin 3 results in bipolar input.

Table 1 – ADC1 configuring information

			Single-ended / Differential		Unipolar / Bipolar	
Analog input	**R_{g1}**	**R_{g2}**	**Closed**	**Open (default)**	**1-2 unip.**	**2-3 bip.**
AIN-1P / AIN-1N	R_{78}	R_{80}	JMP1		JP6 (2-3 default)	
AIN-2P / AIN-2N	R_{83}	R_{85}	JMP2		JP7 (2-3 default)	
AIN-3P / AIN-3N	R_{88}	R_{90}	JMP3		JP8 (2-3 default)	
AIN-4P / AIN-4N	R_{93}	R_{95}	JMP4		JP9 (2-3 default)	
AIN-5P / AIN-5N	R_{110}	R_{112}	JMP5		JP11 (2-3 default)	
AIN-6P / AIN-6N	R_{115}	R_{117}	JMP6		JP12 (2-3 default)	
AIN-7P / AIN-7N	R_{120}	R_{122}	JMP7		JP13 (1-2 default)	
AIN-8P / AIN-8N	R_{125}	R_{127}	JMP8		JP14 (1-2 default)	

Default values are R_{g1}=27.4kΩ, R_{g2}=3.3kΩ with 1% accuracy, resulting in a gain of 0.927[1]. Because of the resulting gain, the full-scale input voltage at the ADC1 connector can be obtained as 5V/0.927≈5.392V.

In order to configure the input scaling stage according to the selected transducer, please refer to **PED-Board_AnalogInputConfig_Rx.y.xlsx**.

ADC output data format is in two-complement, independently from the Unipolar/Bipolar scale selection. Retrieved data specifications are highlighted in Table 2. Accordingly, being the ADC resolution equals to 14-bits, resulting data DB[15:14] are set to zero for positive input voltage and one when negative voltage is applied.

Improved code efficiency and reduced FPGA occupancy can be obtained when 14-bits data input is considered using fixed-point signed data type, avoiding to read DB[15:14].

Table 2 – ADC output data format

Description	**Input voltage value at the ADC input pin**	**Binary and hexadecimal code DB[15:0]**
Positive full scale	+5V	0b ~~00~~01 111 1111 1111 0x 1FFF
Negative full scale	-5V	0b ~~11~~10 0000 0000 0000 0x E000

[1] *Custom configuration available for orders of 5 or more units.*

The pinout of the ADC1 input connector is shown in Figure 4. Each analog input must be connected between the related input P and N. Signal in converted considering the voltage difference P-N (maximum voltage on each pin is 8V).

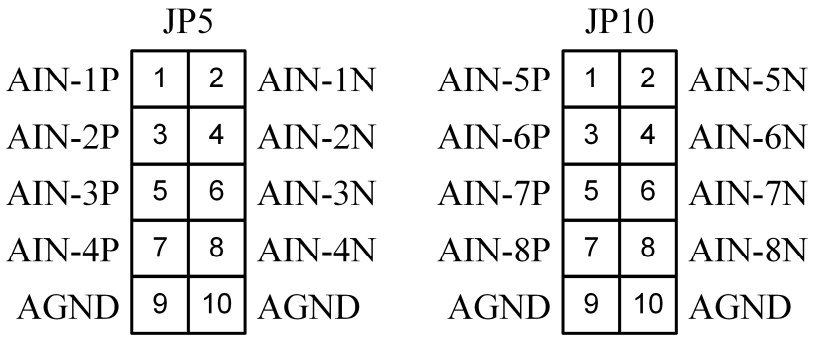

Figure 4. ADC1 connectors.

- *ADC1 filtering section*

Filtering section of ADC1 is accomplished by a II-order low-pass Butterworth type active filter, being based on the well-known multiple-feedback topology. PED-Board is shipped with a filter cut-off frequency set to 20kHz[2].

Please refer to Linear Technologies LT1359CS14 integrated circuit for frequency limitations and detailed filter characteristics.

When the filter cut-off frequency needs to be changed, please refer to the following information that are related to the PED-Board components that must be replaced. Each filter has the scheme shown in Figure 5 whereas the relation between the general element and the PED-Board component designator is reported in Table 3.

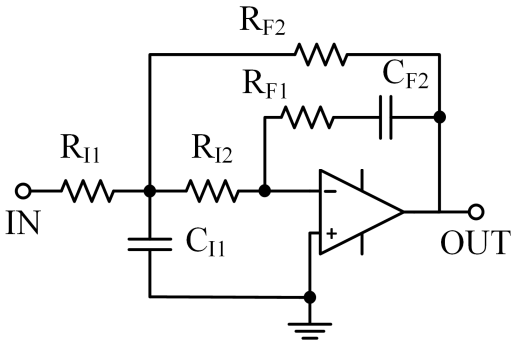

Figure 5. General electrical scheme of the II order Butterworth filter.

Table 3 – Board designators for the filter components

ADC1 channel	R_{I1}	R_{I2}	C_{I1}	R_{F1}	R_{F2}	C_{F2}
AIN-1	R_{97}	R_{99}	C_{139}	Don't change	R_{228}	C_{137}
AIN-2	R_{102}	R_{103}	C_{143}	//	R_{229}	C_{141}
AIN-3	R_{107}	R_{106}	C_{146}	//	R_{231}	C_{142}
AIN-4	R_{101}	R_{100}	C_{140}	//	R_{230}	C_{138}
AIN-5	R_{130}	R_{131}	C_{173}	//	R_{232}	C_{171}
AIN-6	R_{134}	R_{135}	C_{177}	//	R_{233}	C_{175}
AIN-7	R_{139}	R_{138}	C_{180}	//	R_{235}	C_{176}
AIN-8	R_{133}	R_{132}	C_{174}	//	R_{234}	C_{172}

B. ADC2 interface

ADC2 interface is similar to the previously depicted ADC1, except for the low-pass filtering path that is composed by a simple RC filter with impedance matching circuit. Signal conditioning chain is highlighted in Figure 6. Input circuit devoted to scaling and level shifting exhibits the same gain as shown in (1). Each analog input can be configure as single-ended or differential by connecting proper board pads. Moreover, all channels can be configured independently for unipolar or bipolar input. Detailed information are available in Table 4.

[2] *Custom filter configuration available for orders of 5 or more units.*

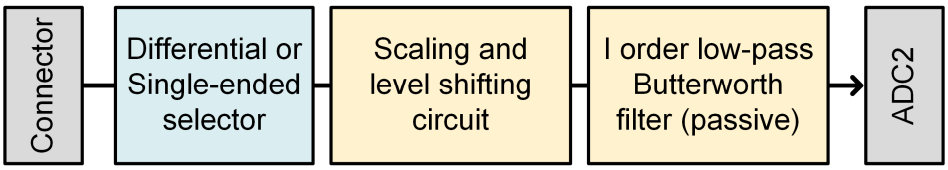

Figure 6. ADC2 measurement chain.

Table 4 – ADC2 configuring information

			Single-ended / Differential		Unipolar / Bipolar	
Analog input	**R_{g1}**	**R_{g2}**	**Closed**	**Open (default)**	**1-2 unip.**	**2-3 bip.**
AIN-9P / AIN-9N	R_{142}	R_{144}	JMP9		JP16 (2-3 default)	
AIN-10P / AIN-10N	R_{147}	R_{149}	JMP10		JP17 (2-3 default)	
AIN-11P / AIN-11N	R_{152}	R_{154}	JMP11		JP18 (2-3 default)	
AIN-12P / AIN-12N	R_{157}	R_{159}	JMP12		JP19 (2-3 default)	
AIN-13P / AIN-13N	R_{162}	R_{164}	JMP13		JP21 (2-3 default)	
AIN-14P / AIN-14N	R_{167}	R_{169}	JMP14		JP22 (2-3 default)	
AIN-15P / AIN-15N	R_{172}	R_{174}	JMP15		JP23 (1-2 default)	
AIN-16P / AIN-16N	R_{177}	R_{179}	JMP16		JP24 (1-2 default)	

Default values are R_{g1}=27.4kΩ, R_{g2}=3.3kΩ with 1% accuracy, resulting in a gain of 0.927.

ADC2 inputs are available on the PED-Board with reference to the pinout shown in Figure 7.

Figure 7. ADC2 connectors.

- *ADC2 filtering section*

ADC2 filtering section is accomplished by a simple first order resistive-capacitive low-pass filter having an impedance matching circuit at its output. Related circuit scheme is shown in Figure 8. Filter cut-off frequency can be selected by choosing the value of the capacitor C_f according to the following expression:

$$F_{coADC2}[Hz] = \frac{1}{2\pi 10^4 C_f[F]} \quad (2)$$

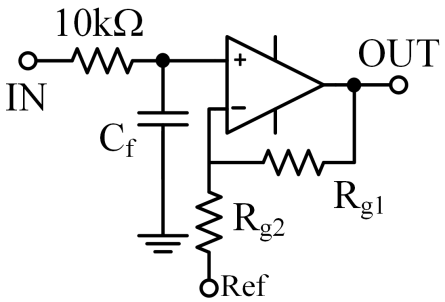

Figure 8. ADC2 filtering and scaling stage.

Filtering capacitor related to each analog input channel is accomplished by the parallel connection of two separated capacitors. PED-Board components designator are reported in Table 5.

Table 5 – ADC filtering capacitor (default: not mounted)[3]

Analog input	C_f	
AIN-9P / AIN-9N	C_{183}	C_{184}
AIN-10P / AIN-10N	C_{191}	C_{192}
AIN-11P / AIN-11N	C_{197}	C_{200}
AIN-12P / AIN-12N	C_{205}	C_{206}
AIN-13P / AIN-13N	C_{215}	C_{216}
AIN-14P / AIN-14N	C_{223}	C_{224}
AIN-15P / AIN-15N	C_{231}	C_{232}
AIN-16P / AIN-16N	C_{235}	C_{240}

C. ADC3 interface

Analog interface ADC3 is capable of low resolution, up to 200kS/s measures acquisition. Digitalization is performed by 10-bit on the available 8 channels. A SPI bus performs communication between the ADC3 and NI sbRIO-9651. ADC3 inputs are available on the JP25 connector having the pinout shown in Figure 9. Analog input voltage swing is unipolar from 0V to +5V. At +5V the resulting output code is 2^{10}-1. No signal conditioning or scaling is provided for ADC3 inputs.

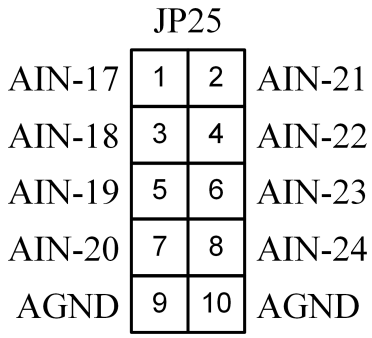

Figure 9. ADC3 connector.

IV. PWM channels (Buffered Digital Outputs)

Up to 30 independent PWM channels are provided through the connectors JP33, JP34, JP35 and JP36 having the detailed pinout of Figure 10. Each channel that is composed by 10 PWM, can be configured to provide 0÷15 V or 0÷5 V voltage swing. When 0÷5V is selected, the PWM pin can drive directly the input LED of a classical opto-coupled gate driver, such as ACPL-333J or HCPL-316.

Voltage selection can be configured by JP2, JP3 and JP4 selectors. Connecting pin 2 to pin 1, each group is supplied from the on-board +5V with 15mA continuous current capability on each PWM output. Whereas connecting pin 2 to pin 3, PWM voltage swing is 0÷15V with 5mA continuous current on each PWM channel. JP2 controls PWM1 to PWM10, JP3 is related to PWM11 to PWM20 and finally JP4 configures PWM21 to PWM30, as summarized in Table 6. PWM buffer circuit is non-inverting.

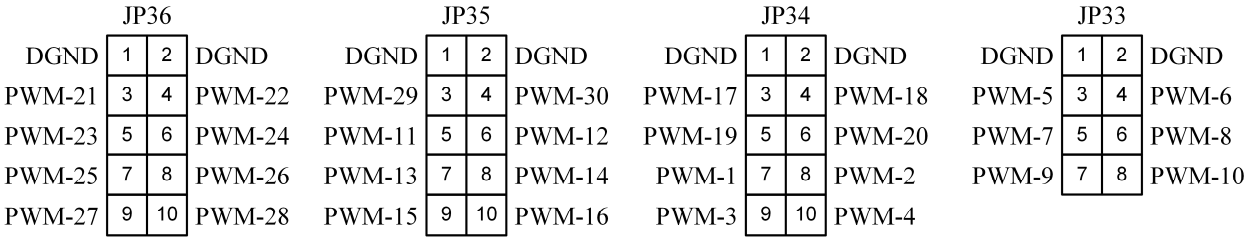

Figure 10. PWM connectors.

[3] *Custom configuration available for orders of 5 or more units.*

Table 6 – PWM voltage swing configuration[4]

	PWM1…PWM10 (JP2)	PWM11…PWM20 (JP3)	PWM21…PWM30 (JP4)
Position 1-2	+5 V (default)	+5 V (default)	+5 V
Position 2-3	+15 V	+15 V	+15 V (default)

Additional PWM outputs can be achieved from the *Digital I/O* pins, implementing the voltage and current driving circuits directly on the application specific Adapter Board.

When each PWM channel needs to be controlled by a dedicated algorithm, NI sbRIO-9651 pins can be directly accessed using the following information (Table 7).

Table 7 – PED-Board and sbRIO-9651 PWM pin routing

PED-Board	sbRIO-9651	PED-Board	sbRIO-9651	PED-Board	sbRIO-9651
PWM-1	DIO_33_N	PWM-11	DIO_31	PWM-21	DIO_56_N
PWM-2	DIO_33	PWM-12	DIO_38_MRCC	PWM-22	DIO_59
PWM-3	DIO_30	PWM-13	DIO_28_N	PWM-23	DIO_59_N
PWM-4	DIO_37_MRCC	PWM-14	DIO_31_N	PWM-24	DIO_62_N
PWM-5	DIO_29	PWM-15	DIO_37_N	PWM-25	DIO_28
PWM-6	DIO_29_N	PWM-16	DIO_39_N	PWM-26	DIO_50_N
PWM-7	DIO_36_SRCC	PWM-17	DIO_34	PWM-27	DIO_53
PWM-8	DIO_36_N	PWM-18	DIO_39_SRCC	PWM-28	DIO_53_N
PWM-9	DIO_32_N	PWM-19	DIO_30_N	PWM-29	DIO_35_N
PWM-10	DIO_32	PWM-20	DIO_34_N	PWM-30	DIO_38_N

V. Digital-to-Analog interface

Digital to analog interface is based on a fast, low settling time converter with SPI interface. Output voltage, which swings from 0V to +5V, is isolated from the board ground, allowing to drive directly any output circuit avoiding ground loops. DAC resolution is 12 bit, starting from 0 to 4095 where the full output voltage is available. DAC connector shown in Figure 11 provide also one isolated digital output channel, DO-ISO. DAC and DO-ISO are on the same ground.
For faster usage of the DAC outputs, even with reduced channels, the connector shown in Figure 12 is provided. Mate connector DIGIKEY code ED10556-ND.

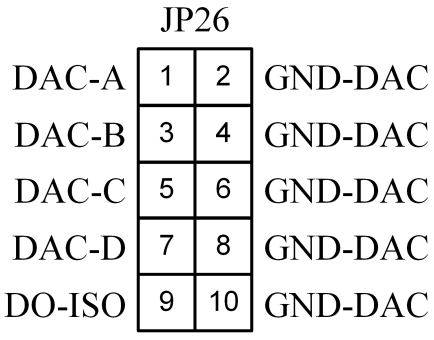

Figure 11. Connector for DAC and Digital-Out pin.

Figure 12. Fast DAC connector.

[4] *Custom configuration available for orders of 5 or more units.*

VI. Resolver interface

Resolver interface is mainly based on the Analog Devices AD2S1205YST integrated circuit. Differential excitation is provided with on-board current buffer. Sin/Cos acquiring circuits are designed to accomplish different type of resolvers, being equipped with a dedicated scaling circuit that can be configured by simply replacing some resistors. Carrier signal amplitude regulation is also allowed with a maximum peak voltage of 10V. Excitation driving circuit is able to directly supply resolvers based on rotary transformer or switched reluctance architecture. Scheme of the excitation circuit is shown in Figure 13 and it is reported in [1]. Both carrier signals, EXE+ and EXE- have the same amplification circuit. Detailed information on how to select the circuit component can be found in [1]. Resolver Sin/Cos acquiring circuit is shown in Figure 14, where three input resistors can be used to properly scale the resolver return signals. With reference to the PED-Board, Sin signal resistors are R_{s1}=R_{182}, R_{s2}=R_{183} and R_{s3}=R_{186}. Accordingly, Cos resistors are R_{s1}=R_{191}, R_{s2}=R_{192} and R_{s3}=R_{195}. More info can be found on Table 8 where the default values are also indicated. If the component value is not specified it stands for 'not mounted'. Resolver signals can be accessed by the JP27 connector as shown in Figure 15.

Table 8 – Resolver circuit components[5]

	EXE+	EXE-		Sin	Cos
R_{e1}	R_{197} (24 kΩ)	R_{199} (24 kΩ)	R_{s1}	R_{182} (5.6 kΩ)	R_{191} (5.6 kΩ)
R_{e2}	R_{236} (15 kΩ)	R_{238} (15 kΩ)	R_{s2}	R_{183} (12 kΩ)	R_{192} (12 kΩ)
R_{b1}	R_{241} (12 kΩ)		R_{s3}	R_{186} (5.6 kΩ)	R_{195} (5.6 kΩ)
R_{b2}	R_{243} (27 kΩ)				
C_{e1}	C_{324}	C_{325}			
R_{f1}	R_{239}	R_{240}			
C_{f1}	C_{327}	C_{328}			
R_{fo}	R_{237}				
C_{fo}	C_{326}				

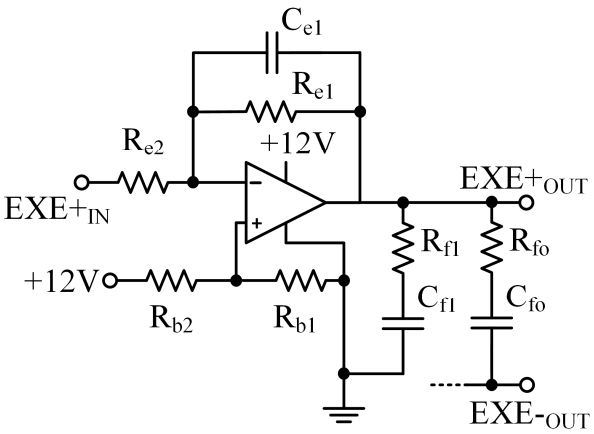

Figure 13. Electrical scheme of the resolver excitation circuit.

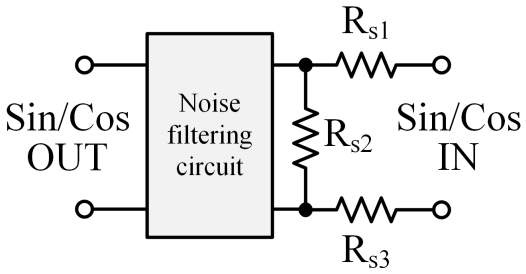

Figure 14. Resolver Sin/Cos scaling and acquiring circuit.

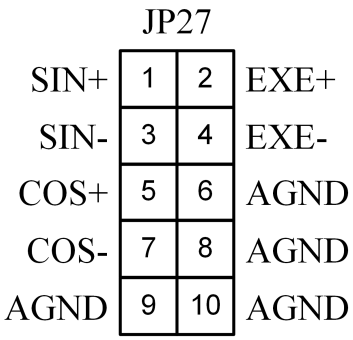

Figure 15. Resolver connector.

[5] *Custom resolver configuration available for orders of 5 or more units.*

VII. CAN-bus

Isolated CAN transceiver having an operating data rate up to 1 Mbit/s has been integrated on the PED-Board. LabVIEW CLIP can straightforwardly realize the CAN controller if needed. However, it takes some FPGA resources resulting in an average estimation around 5.9% of Slice Registers, 12.5% of Slice LUTs and 10% of Block RAMs. No DSP48s resources are taken to implement the CAN controller. CAN connector is provided as shown in Figure 16. Mate connector DIGIKEY code ED10556-ND.

Figure 16. Fast CAN-bus connector

When CAN communication is not needed, FPGA space can be saved by removing the CAN controller from the generated CLIP.

CLIP generation requires the information concerning the sbRIO-9651 pins to be used as CAN TX and RX. Provided PED-Board CAN controller is connected as in Table 9.

Table 9 - Pin routing between the CAN-Bus transceiver and the sbRIO-9651

PED-Board	sbRIO-9651
CAN_TX	DIO_8
CAN_RX	DIO_9

R213 is used to setup the slope of the CAN-bus data (default 0 Ω). 120 Ω termination resistor can be inserted if needed, by closing the jumper JCAN.

- *II CAN controller*

A second CAN-bus controller can be implemented by the LabVIEW CLIP generator and it will be available to the Digital I/O pins. The required transceiver can be placed directly on the *Adapted Board*.

VIII. RS-485

RS-485 port can be generated by the LabVIEW CLIP Generator. PED-Board is equipped with an isolated transceiver and a dedicated connector M3 having the pinout shown in Figure 17.

RS-485 CLIP can be generated according to the pin routing shown in Table 10.

Each TX and RX channel has its own 120 Ω termination resistor, which can be inserted by closing the jumper J485-H for RX and J485-F for TX. In case of half-duplex mode of operation, only one termination resistor should be closed.

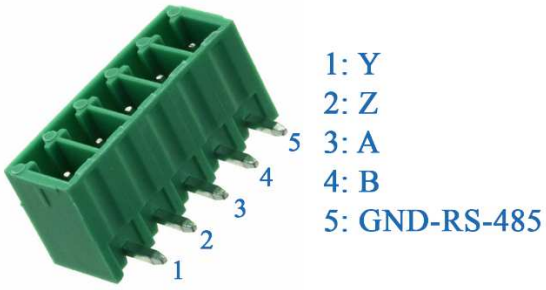

Figure 17. RS-485 connector.

Table 10 – Pin routing between the RS-485 transceiver and the sbRIO-9651

PED-Board	sbRIO-9651	
RS485_TX_EN	DIO_11	Transceiver TX enable pin
RS485_TX	DIO_12	Transceiver TX pin
RS485_RX	DIO_14	Transceiver RX pin
RS485_RX_EN	DIO_15_MRCC	Transceiver RX enable pin

IX. Digital I/O

Additional I/O pins are available through JP29, JP30, JP31 and JP32 connectors that allow to route those pins directly to the *Adapter Board*. Connectors' pinout is highlighted in Figure 18. Digital I/O are directly connected to the ZYNQ-7020 pins, refers to the Xilinx device data-sheet for the electrical specifications.

Provided additional Digital I/O pins are directly connected to the sbRIO-9651 FPGA pins. According to the National Instruments sbRIO-9651 data-sheet, the relation between the PED-Board and sbRIO-9651 pins is as in Table 11.

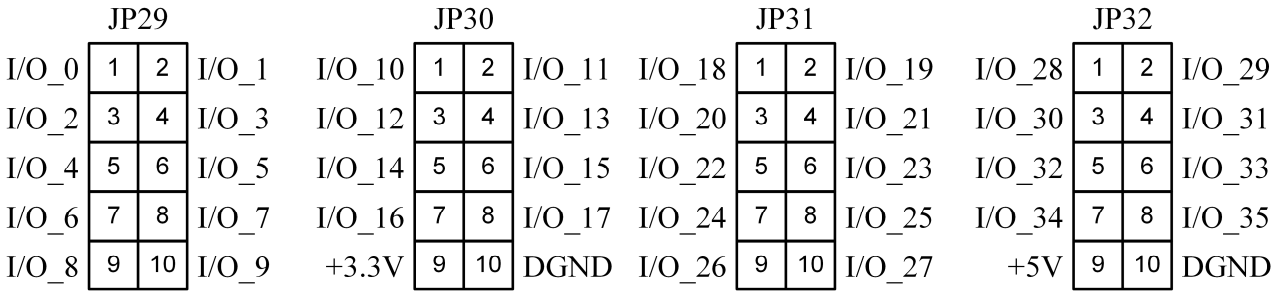

Figure 18. Digital I/O connectors.

Table 11. PED-Board vs. sbRIO-9651 digital I/O pins

PED-Board	sbRIO-9651	PED-Board	sbRIO-9651	PED-Board	sbRIO-9651	PED-Board	sbRIO-9651
I/O_0	DIO_25_N	I/O_10	DIO_23_N	I/O_18	DIO_48	I/O_28	DIO_70_N
I/O_1	DIO_0	I/O_11	DIO_21_N	I/O_19	DIO_44	I/O_29	DIO_67_N
I/O_2	DIO_25	I/O_12	DIO_24	I/O_20	DIO_48_N	I/O_30	DIO_71
I/O_3	DIO_1	I/O_13	DIO_21	I/O_21	DIO_45_N	I/O_31	DIO_67
I/O_4	DIO_22	I/O_14	DIO_24_N	I/O_22	DIO_49	I/O_32	DIO_71_N
I/O_5	DIO_19	I/O_15	DIO_43_N	I/O_23	DIO_45	I/O_33	DIO_68_N
I/O_6	DIO_22_N	I/O_16	DIO_47	I/O_24	DIO_49_N	I/O_34	DIO_72
I/O_7	DIO_20_N	I/O_17	DIO_43	I/O_25	DIO_46_N	I/O_35	DIO_68
I/O_8	DIO_23			I/O_26	DIO_70		
I/O_9	DIO_20			I/O_27	DIO_46		

D. Hall sensors interface and Encoder port

PED-Board is equipped with a digital interface for glue less connection of low-resolution hall-effect position sensors. These can be connected to the pins provided by the Digital I/O port, JP29, JP30, JP31 and JP32. As shown in Figure 18, non-isolated +3.3V and +5V auxiliary supplies are provided, which can be used to directly fed hall-sensors and encoders with a maximum available current of 100mA for each one.

X. Status and User LEDs, User button and Reset, USB port

PED-Board is equipped with three LEDs related to the sbRIO-9651 operation, POWER (green), STATUS (yellow) and TEMP (red). Please refer to the National Instruments System-On-Module data-sheet for detailed explanation.

Additional user LEDs are provided, which can be controlled directly from the sbRIO-9651: LED1 (green) connected to the pin DIO_75 and LED2 (green) connected to DIO_81.

NI sbRIO-9651 can be reset by pressing SW1. SW2 can be used as user switch, having normally low state. It is connected to the DIO_87_SRCC pin of the sbRIO-9651 board.

USB port, formally USB1, can act only as HOST port.

XI. Mechanical dimensions

PED-Board size is 220mm x 130mm.

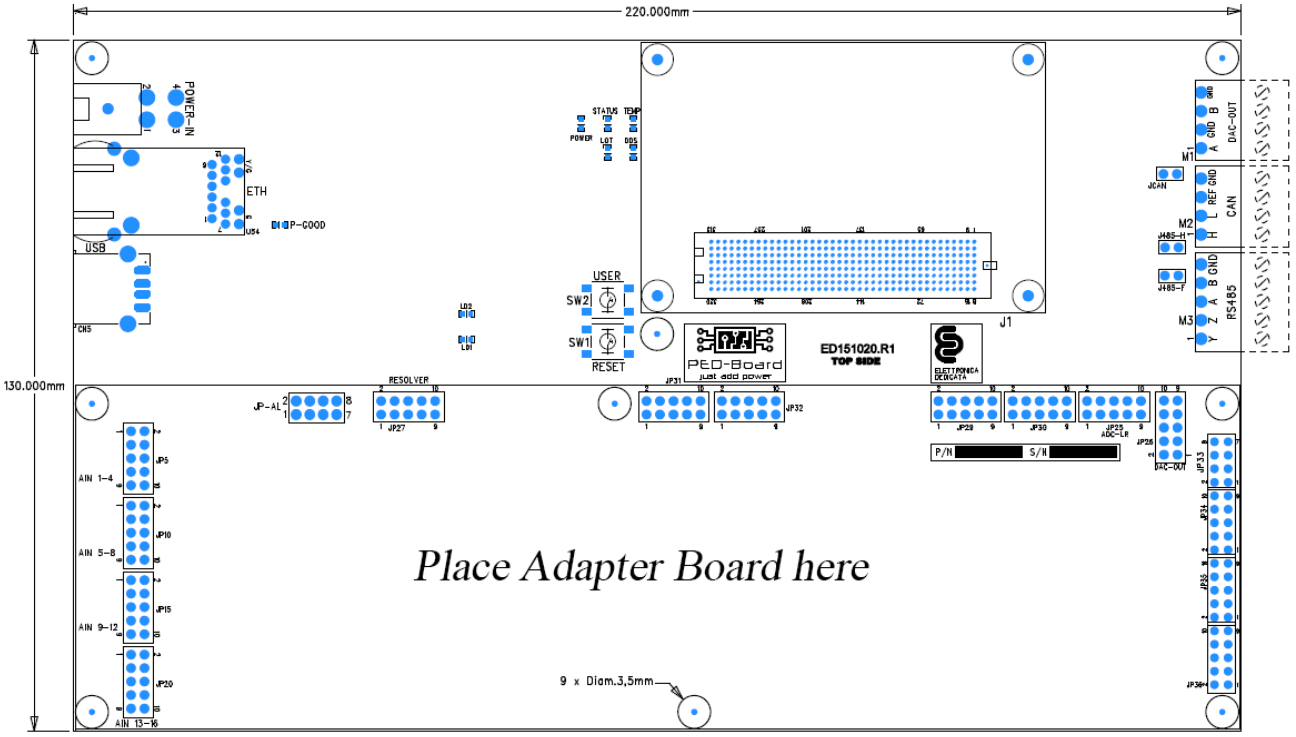

Figure 19. PED-Board mechanics.

Detailed mechanical information can be found in **PED-Board_Specs_Mech.dxf**, which is available on-line in the download section.

Application specific Adapter Board must be placed above the board-to-board connectors, i.e. in the PED-Board bottom rectangle shown in Figure 19.

XII. References

[1] Jakub Szymczak, Shane O'Meara, Johnny S. Gealon, and Christopher Nelson De La Rama, "Precision Resolver-to-Digital Converter Measures Angular Position and Velocity", Analog Devices application note.

XIII. Revision history

Date	Rev #	
2017-05-30	1.06	ADC1 and ADC2 input scale and gain have been explained and updated.
2017-01-25	1.05	Functional block diagram updated, DAC was reported having 10bit resolution instead of 12bit.
2016-04-28	1.04	PED-Board picture updated, pag. 3.
2016/04/20	1.03	Figure 4, Figure 7, Figure 9, Figure 10, Figure 11, Figure 15, Figure 18 have been updated: pin 5 was named pin 4, resulting is two pin 4. *Critical update*: pinout of connectors in Figure 10 has been updated. Table 1 and Table 4 default configuration updated.
2016/04/01	1.02	Contacts added. HUM exits preliminary state.
2016/02/28	1.01	Figure 10 has been updated. Custom configuration footnotes added.

Contacts

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